

**What is claimed is:**

1. A simulation apparatus that is intended for a very long instruction word processor, comprising:

a first simulation unit operable to simulate execution of a group of instructions to be executed simultaneously; and

a second simulation unit operable to generate a simulation result of the group of instructions on an instruction-by-instruction basis based on a simulation result generated by the first simulation unit.

2. The simulation apparatus according to Claim 1, wherein the second simulation unit generates a simulation result by undoing a simulation of an instruction included in a group of instructions that has just been simulated by the first simulation unit.

3. The simulation apparatus according to Claim 2 further comprising:

a display control unit operable to control a display unit to display the simulation result generated by the second simulation unit.

4. The simulation apparatus according to Claim 2, wherein the second simulation unit includes:

a judgment unit operable to judge whether an instruction that satisfies a break condition is included in the group of instructions that has just been simulated by the first simulation unit or not;

an indication unit operable to indicate that the first simulation unit simulates execution of a next group of instructions when it is judged that no instruction satisfying the break condition is included;

a determination unit operable to determine an instruction as a stop instruction when it is judged that the instruction satisfying

the break condition is included; and

a generation unit operable to generate a simulation result by undoing simulations of the stop instruction and the following instructions in the group of instructions that have just been simulated.

5. The simulation apparatus according to Claim 1, wherein the first simulation unit is intended for a pipeline processor that executes a plurality of instructions simultaneously, the simulation apparatus further comprises:

a display image generation unit operable to generate a display image showing instructions that are included in a pipeline based on simulation results generated by the first simulation unit and the second simulation unit.

6. The simulation apparatus according to Claim 5, wherein the display image contains representation of an instruction that is included in every stage of the pipeline.

7. The simulation apparatus according to Claim 1, wherein the first simulation unit simulates, on a cycle-by-cycle basis, operations of a pipeline processor that executes a plurality of instructions simultaneously, the simulation apparatus further comprises:

an acceptance unit operable to accept a user operation that indicates one of a step execution performed on an instruction-by-instruction basis and a step execution performed on a cycle-by-cycle basis; and

a display image generation unit operable to generate a display image that shows a simulation result generated on an instruction-by-instruction basis by the second simulation unit when a user operation that indicates a step execution performed on an

instruction-by-instruction basis is accepted and to generate a display image that shows a simulation result generated on a cycle-by-cycle basis by the first simulation unit when a user operation that indicates a step execution performed on a cycle-by-cycle basis is accepted.

8. The simulation apparatus according to Claim 7, wherein the display image contains representation of each instruction that is included in a pipeline.

9. The simulation apparatus according to Claim 7, wherein the display image contains representation of instructions that is included in every stage of a pipeline.

10. The simulation apparatus according to Claim 1, wherein the first simulation unit includes:  
a hold unit operable to hold first data showing resources of the very long instruction word processor;  
a storage unit operable to store a copy of the first data in the memory unit as second data; and  
a first simulator that updates the first data by simulating an execution of a single group of instructions after storing the copy, and wherein the second simulation unit obtains simulation results of the group of instructions on an instruction-by-instruction basis based on the first data and the second data.

11. The simulation apparatus according to Claim 10, wherein the storage unit stores data of a register set in the memory unit as the second data, and  
the second simulation unit reconstructs data of the resource before executing a simulation of the instruction of the group of instructions on an instruction-by-instruction basis.

12. The simulation apparatus according to Claim 11,  
wherein the storage unit further stores memory data before  
memory writing in the hold unit in a way that said memory data is  
contained in the second data when a memory write instruction is  
5 included in the group of instructions.

13. The simulation apparatus according to Claim 10,  
wherein the second simulation unit includes:

a judgment unit operable to judge whether an instruction that  
10 satisfies a break condition is included in the group of instructions  
that has just been simulated by the first simulation unit or not;

an indication unit operable to indicate that the first simulation  
unit simulates execution of a next group of instructions when it is  
judged that no instruction satisfying the break condition is included;

15 and

a determination unit operable to determine an instruction  
that satisfies the break condition as a stop instruction when it is  
judged that the instruction satisfying the break condition is  
included.

14. The simulation apparatus according to Claim 13,  
wherein the determination unit determines an instruction  
next to a present stop instruction as a break condition in the step  
execution of a simulation performed on an instruction-by-instruction  
25 basis.

15. The simulation apparatus according to Claim 13,  
wherein the second simulation unit further includes:

a reconstruction unit operable to reconstruct, based on the  
30 first data and the second data, data of resources on condition that  
instructions up to an instruction just before the stop instruction  
determined by the determination unit are simulated.

16. The simulation apparatus according to Claim 13,  
wherein the second simulation unit further includes:

a reconstruction unit operable to reconstruct, based on the first data and the second data, data of resources on condition that instructions up to the stop instruction determined by the determination unit are simulated.

17. The simulation apparatus according to Claim 16,

wherein the first simulator generates update information showing resources to be changed by each instruction of the group of instructions, and

the reconstruction unit reconstructs the data of resources corresponding to sequential execution results of the instructions up to each instruction of the group of instructions according to the first data, the second data and update information.

18. The simulation apparatus according to Claim 10,

wherein the first simulator simulates execution of the group of instructions on a cycle-by-cycle basis of pipeline processing, the first simulator being intended for the very long instruction word processor that executes the pipeline processing, and

the simulation apparatus further counts the number of execution cycles in the simulation for every group of instructions.

19. The simulation apparatus according to Claim 18,

wherein the very long instruction word processor has a cancellation unit for canceling execution of an instruction in a plurality of instructions to be executed simultaneously, and the first simulator simulates the cancellation unit.

20. The simulation apparatus according to Claim 18,

wherein the first simulator further simulates a delay cycle as

to a delay instruction that causes a delay cycle in an execution stage of the very long instruction word processor to be simulated, and  
the reconstruction unit generates data of resources corresponding to a simulation result of a delay instruction according  
5 to update information on the delay instruction.

21. The simulation apparatus according to Claim 20,  
wherein the reconstruction apparatus further generates data of resources corresponding to a simulation result of an output  
10 dependency instruction according to the update information on the delay instruction and the update information on the output dependency instruction as to the output dependency instruction that has output dependency in the same group of instructions with the delay instruction.

22. A simulation method that is intended for a very long instruction word processor, comprising:

the first step of simulating execution of a group of instructions comprising a plurality of instructions to be executed  
20 simultaneously, and

the second step of generating a simulation result of the group of instructions on an instruction-by-instruction basis based on a simulation result in the first step.

23. A program for having a computer execute a simulation of a very long instruction word processor, the program has the computer execute the following steps:

the first step of simulating execution of a group of instructions comprising a plurality of instructions to be executed  
30 simultaneously, and

the second step of generating a simulation result of the group of instructions on an instruction-by-instruction basis based on a

simulation result in the first step.

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